

Notice of Allowability

Application No.

09/475,717

Examiner

Dwin M Craig

Applicant(s)

NARDIN ET AL.

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 5-19-2004.
2. ☒ The allowed claim(s) is/are 1,3-6,8-12,14-18,20,22,24 and 26, now renumbered as 1-19-
3. ☒ The drawings filed on 04 March 2003 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) ✓
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

JEAN P. HOMERE
PRIMARY EXAMINER

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DETAILED ACTION

And

NOTICE of ALLOWANCE

1. Claims 1, 3, 4, 5, 6, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 20, 22, 24 and 26 are allowed.

Claims 2, 7, 13, 19 and 23 have been cancelled.

Affidavit

2. Regarding Applicants submission of an affidavit under 37 C.F.R. 1.131:

Applicant's affidavit submitted on 5-19-2004 has been considered persuasive and overcomes the 35 U.S.C. 103(a) rejections applied by the Examiner to Independent Claims 1, 4, 10, 15 and 17. Specifically, Applicant's affidavit discloses that the limitation of "*indicating whether any of the domino logic circuits is likely to generate an erroneous output*" is disclosed in; *Exhibit C, page 2 Lines 3: The portion "+0.048V DYNOUT" indicates that the particular domino circuit simulated has a positive noise margin and therefore has a low likelihood to generate an erroneous output*, as sworn to by the Applicant on page 3 of the affidavit under 37 C.F.R. 1.131 recorded on 4-21-2004.

Examiner's reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

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3.1 The prior art, in view of Applicant's affidavit and instant amendments to the claim language, does not explicitly teach or render obvious the claimed limitations as recited in Claims 1, 4, 10, 15 and 17.

Independent **Claims 1, 4, 10, 15 and 17** recite limitations in combination with the following limitations: "*simulating each domino logic circuit*" and "*reporting results of the simulating indicating whether any of the domino logic circuits is likely to generate an erroneous output*" which provide a patentable distinction over the prior art. Further, as shown in the prior art, specifically in the *Sinha* reference and in the *Heikes et al. U.S. Patent 5,798,938* the term *erroneous output* is clearly defined to mean, "...the clocks n and $n+1$ can be offset only as much as T_p , but no more, or the logic circuit may produce erroneous outputs because the data read by clock $n+1$ has been prematurely pre-charged away. (*Heikes et al. Col. 8 Lines 12-23*). Erroneous outputs meaning, unintended or incorrect logic conditions or states, in this case coming out of a domino circuit, as opposed to correctly decoded logic control signals resulting from correct decoding of inputs to a domino circuit. The prior art discloses methods of simulating domino circuits, and methods of avoiding *erroneous outputs* however, the prior art does not expressly teach or make obvious, the method of, *simulating a domino circuit* and then *indicating* if that simulated domino circuit will have an erroneous output, as argued by the Applicant.

In the response to the September 29, 2003 office action Applicant argued, "*In light of the enclosed Declaration, Sinha may not be relied upon as prior art under 103(a). Since the Examiner acknowledges that, the Rajgopal et al. reference does not expressly disclose the limitation concerning analysis of domino circuits wherein each domino circuit is simulated in a*

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specific order and the next domino circuit is analyzed using as an input the output of the last domino circuit that was analyzed and reporting results of the simulation indicating whether any of the domino logic circuits are likely to generate an erroneous output", page 3 of Applicants response of 5-17-2004. These arguments, in combination with the instant amendments to independent claims 1, 4, 10, 15 and 17 and in combination with the Affidavit filed under 37 C.F.R. 1.131 have been in combination with Applicant's admittance and interpretation of the prior art asserted, considered persuasive so as to overcome the prior art.

3.2 As regards independent **Claim 17** it is noted that the Applicant has invoked 35 U.S.C. 112 6th paragraph with the use of *means for* language. The Examiner notes that the Applicant draws structural support for *extracting parameters* from Figure 4A item 400 and 4B item 470, and page 12 of the specification. The Examiner notes that the Applicant draws structural support for *scheduling the set of domino logic circuits into an ordered list* from Figures 4A and 4B and from page 12 of the specification. The Examiner notes that the Applicant draws structural support for *simulating each domino circuit* from Figure 4A item 420 and pages 12-15. The Examiner notes that the Applicant draws structural support for *reporting results* from Figure 6 Item 640 "*Master Report Generator*" and page 15 of the specification.

3.3 Dependent **Claims 3, 5, 6, 8, 9, 11, 12, 14, 16, 18, 20, 22, 24 and 26** are allowed as they depend upon an allowed base claim.

3.4 Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Claims 1, 3, 4, 5, 6, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 20, 22, 24 and 26 are allowed.

4.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The IEEE paper entitled, "Charge Sharing Fault Detection for CMOS Domino Logic Circuits" by C.H. Cheng, S.C. Chang, J.S. Wang and W.B. Jone discloses domino logic circuit configurations that can create erroneous outputs.

4.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwain M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC


JEAN R. HOMERE
PRIMARY EXAMINER